CLAIMS

1. A semiconductor structure comprising:

a first semiconductor layer having a plurality of threading dislocations distributed substantially uniformly across a surface thereof; and

a compositionally uniform cap layer disposed over the surface of the first layer, the cap layer being substantially relaxed.

2. The semiconductor structure of claim 1 wherein a lattice constant of the compositionally uniform cap layer is different from a lattice constant of the first layer.

3. The semiconductor structure of claim 1 further comprising:
a strained semiconductor layer disposed over the compositionally uniform cap layer.

4. The semiconductor structure of claim 3 wherein the strained semiconductor layer is tensilely strained.

5. The semiconductor structure of claim 4 wherein the strained semiconductor layer comprises tensilely strained silicon or tensilely strained silicon-germanium alloy.

6. The semiconductor structure of claim 3 wherein the strained semiconductor layer is compressively strained.

7. The semiconductor structure of claim 6, wherein the strained semiconductor layer comprises compressively strained germanium or compressively strained silicon-germanium alloy.

8. The semiconductor structure of claim 1 wherein the compositionally uniform cap layer comprises at least one of a group II, a group III, a group IV, a group V, and a group VI element.

9. The semiconductor structure of claim 8 wherein the compositionally uniform cap layer comprises at least one of silicon and germanium.

10. The semiconductor structure of claim 9 wherein the compositionally uniform cap layer comprises more than approximately 10% germanium.

11. The semiconductor structure of claim 1 wherein the thickness of the compositionally uniform cap layer ranges from about 0.5 μm to about 3.0 μm.

12. The semiconductor structure of claim 1 wherein the compositionally uniform cap is planarized.

13. The semiconductor structure of claim 1 further comprising:
a compositionally graded layer disposed between the compositionally uniform cap layer and the first layer.

14. The semiconductor structure of claim 13 wherein the graded layer comprises at least one of a group II, a group III, a group IV, a group V, and a group VI element.

15. The semiconductor structure of claim 14 wherein the graded layer comprises at least one of silicon and germanium.

16. The semiconductor structure of claim 15 wherein the graded layer has a grade rate greater than about 5% germanium per micrometer.

17. The semiconductor structure of claim 16 wherein the graded layer has a grade rate less than about 50% germanium per micrometer.

18. The semiconductor structure of claim 13 wherein the graded layer is graded to a concentration of greater than about 10% germanium.

19. The semiconductor structure of claim 13 wherein the thickness of the graded layer ranges from about 0.5 μm to about 10.0 μm.

20. The semiconductor structure of claim 13 wherein the first layer comprises an initial portion of the graded layer; the initial portion having a lower local grading rate than at least one subsequent portion of the graded layer and wherein the threading dislocations are uniformly distributed in the initial portion.

21. The semiconductor structure of claim 20 wherein the graded layer comprises at least one of silicon and germanium.

22. The semiconductor structure of claim 21 wherein the difference in local grading rate is greater than about 5% Ge/μm.

23. The semiconductor structure of claim 22 wherein the difference in local grading rate is greater than about 20% Ge/μm.

24. The semiconductor structure of claim 21 wherein the grading rate of the initial portion of the relaxed graded buffer layer does not exceed about 10% Ge/μm.

25. The semiconductor structure of claim 21 wherein the discontinuity in Ge content at the interface between the initial portion and at least one subsequent portion of the relaxed graded layer does not exceed about 10% Ge.

26. The semiconductor structure of claim 25 wherein the discontinuity in Ge content at the interface between the initial portion and at least one subsequent portion of the relaxed graded buffer layer does not exceed about 5% Ge.

27. The semiconductor structure of claim 1 wherein the first layer comprises a seed layer disposed proximal to the surface of the first layer and wherein the threading dislocations are uniformly distributed in the seed layer.

28. The semiconductor structure of claim 27 wherein the seed layer is at least partially relaxed.

29. The semiconductor structure of claim 27 wherein the seed layer is compositionally uniform.

30. The semiconductor structure of claim 27 wherein the seed layer is compositionally graded.

31. The semiconductor structure of claim 27 wherein the thickness of the seed layer is greater than twice its equilibrium critical thickness.

32. The semiconductor structure 31 wherein the thickness of the seed layer is less than about five times its equilibrium critical thickness.

33. The semiconductor structure 27 wherein at least a portion of the seed layer is formed by growth at a growth temperature of about 850°C.

34. The semiconductor structure 27 wherein at least a portion of the seed layer is formed by growth at a growth temperature above 1000 °C.

35. The semiconductor structure 27 wherein the seed layer has a thickness ranging from about 10 nm to about 1000 nm.

36. The semiconductor structure 35 wherein the seed layer has a thickness ranging from about 30 nm to about 300 nm.

37. The semiconductor structure 27 wherein the cap layer has a density of dislocation pile-ups of less than about 1/cm.

38. The semiconductor structure 27 wherein the cap layer has a density of dislocation pile-ups of less than 0.01/cm.

39. The semiconductor structure 27 wherein the cap layer has a threading dislocation density of less than about $5 \times 10^5/cm^2$.

40. The semiconductor structure of claim 27, further comprising:
a compositionally uniform buffer layer disposed between the compositionally uniform cap layer and the seed layer.

41. The semiconductor structure of claim 40 wherein the buffer layer comprises silicon.

42. The semiconductor structure of claim 40 wherein at least one of the buffer layer and the seed layer comprises at least one of silicon and germanium.

43. The semiconductor structure of claim 42 wherein a concentration of germanium in the buffer layer is different than a concentration of germanium in the seed layer at an interface between the seed layer with the buffer layer.

44. The semiconductor structure of claim 43 wherein discontinuity in germanium concentration at an interface between the seed layer with the buffer layer ranges from about 2% to 50% Ge.

45. The semiconductor structure of claim 44 wherein discontinuity in germanium concentration at an interface between the seed layer with the buffer layer ranges from about 5% to 15% Ge.

46. The semiconductor structure of claim 45 wherein discontinuity in germanium concentration at an interface between the seed layer with the buffer layer comprises about 10% Ge.

47. The semiconductor structure of claim 27, further comprising a compositionally graded layer disposed between the compositionally uniform cap layer and the seed layer.

48. The semiconductor structure of claim 47 wherein at least one of the graded layer and the seed layer comprises at least one of silicon and germanium.

49. The semiconductor structure of claim 47 wherein a concentration of germanium in the graded layer is different from a concentration of germanium in the seed layer at an interface between the seed layer with the graded layer.

50. The semiconductor structure of claim 49 wherein discontinuity in germanium concentration at an interface between the seed layer with the graded layer ranges from about 2% to 50% Ge.

51. The semiconductor structure of claim 50 wherein discontinuity in germanium concentration at an interface between the seed layer with the graded layer ranges from about 5% to 15% Ge.

52. The semiconductor structure of claim 51 wherein discontinuity in germanium concentration at an interface between the seed layer with the graded layer comprises about 10% Ge.

53. The semiconductor structure of claim 47, further comprising at least one intermediate seed layer disposed within the graded layer.

54. The semiconductor structure of claim 1 wherein the first layer comprises a silicon-on-insulator substrate.

55. A method of fabricating a semiconductor structure having reduced threading dislocation pile-ups, the method comprising:

providing a first semiconductor layer having a plurality of threading dislocations distributed substantially uniformly across a surface thereof; and

forming a compositionally uniform cap layer over the surface of the first semiconductor layer, the cap layer being substantially relaxed, the first

semiconductor layer inhibiting formation of dislocation pile-ups in at least the cap layer.

56. The method of claim 55 wherein a lattice constant of the compositionally uniform cap layer is different from a lattice constant of the first layer.

57. The method of claim 55, further comprising, prior to forming the cap layer, forming a compositionally uniform buffer layer over the first layer.

58. The method of claim 55 wherein the step of providing a first semiconductor layer comprises forming an at least partially relaxed seed layer over a semiconductor substrate.

59. The method of claim 58 wherein the step of forming the at least partially relaxed seed layer comprises growing the seed layer to a thickness ranging between two and five times an equilibrium critical thickness of the seed layer.

60. The method of claim 58 wherein the step of forming the at least partially relaxed seed layer comprises annealing the seed layer at a temperature above the deposition temperature thereof.

61. The method of claim 55 wherein the step of providing a first semiconductor layer comprises implanting a species into the first semiconductor layer.

62. The method of claim 61 wherein the first semiconductor layer comprises silicon and the species comprises silicon.

63. The method of claim 55 wherein the step of providing a first semiconductor layer comprises providing a semiconductor-on-insulator substrate.

64. The method of claim 55 wherein the step of providing the first semiconductor layer comprises providing a silicon substrate having a substantially uniform distribution of threading dislocations.

65. The method of claim 55 wherein the step of providing the first semiconductor layer comprises providing a silicon substrate having a density of threading dislocations in excess of about 10^2 /cm^2.

66. The method of claim 55 wherein the step of providing the first semiconductor layer comprises providing a silicon substrate having a density of threading dislocations in excess of about 10^3 /cm^2.

67. The method of claim 55 wherein the step of providing the first semiconductor layer comprises providing a silicon substrate having a density of threading dislocations in excess of about 10^4 /cm^2.

68. The method of claim 55 wherein the step of providing the first semiconductor layer comprises providing a silicon substrate having an average surface roughness greater than 1Å.

69. The method of claim 55 wherein the step of providing the first semiconductor layer comprises providing a silicon substrate having an average surface roughness greater than 5Å.

70. The method of claim 55 wherein the cap layer has a density of dislocation pile-ups of less than 1/cm.

71. The method of claim 55 wherein the cap layer has a density of dislocation pile-ups of less than 0.01/cm.

72. The method of claim 55 wherein the cap layer has a threading dislocation density of less than about 5×10^5/cm^2.

73. The method of claim 55, further comprising:
forming a compositionally graded layer prior to forming the cap layer.

74. The method of claim 73, further comprising forming at least one seed layer within the compositionally graded buffer layer.

75. A semiconductor structure comprising:

a first semiconductor layer having a plurality of threading dislocations distributed substantially uniformly across a surface thereof;

a compositionally uniform cap layer disposed over the surface of the first layer, the cap layer being substantially relaxed; and

a p-type metal-oxide-semiconductor (PMOS) transistor disposed over the relaxed cap layer, the PMOS transistor including:

a gate dielectric portion disposed over a portion of the relaxed cap layer,

a gate disposed over the gate dielectric portion, the gate comprising a conducting layer, and

a source and a drain disposed proximate the gate dielectric portion, the source and first drain including p-type dopants.

76. A semiconductor structure comprising:

a first semiconductor layer having a plurality of threading dislocations distributed substantially uniformly across a surface thereof;

a compositionally uniform cap layer disposed over the surface of the first layer, the cap layer being substantially relaxed; and

an n-type metal-oxide-semiconductor (NMOS) transistor disposed over the relaxed cap layer, the NMOS transistor including:

a gate dielectric portion disposed over a portion of the relaxed cap layer,

a gate disposed over the gate dielectric portion, the gate comprising a conducting layer,

a source and a drain disposed proximate the gate dielectric portion, the source and drain including n-type dopants.

77. A semiconductor structure comprising:

a first semiconductor layer having a plurality of threading dislocations distributed substantially uniformly across a surface thereof;

a compositionally uniform cap layer disposed over the surface of the first layer, the cap layer being substantially relaxed;

a p-type metal-oxide-semiconductor (PMOS) transistor disposed over the relaxed cap layer, the PMOS transistor including:

a first gate dielectric portion disposed over a first portion of the relaxed cap layer,

a first gate disposed over the first gate dielectric portion, the first gate comprising a first conducting layer,

a first source and a first drain disposed proximate the first gate dielectric portion, the first source and first drain including p-type dopants; and

an n-type metal-oxide-semiconductor (NMOS) transistor disposed over the relaxed cap layer, the NMOS transistor including:

a second gate dielectric portion disposed over a second portion of the relaxed cap layer,

a second gate disposed over the second gate dielectric portion, the second gate comprising a second conducting layer,

a second source and a second drain disposed proximate the second gate dielectric portion, the second source and second drain including n-type dopants.

78. The semiconductor structure of claim 1 wherein the compositionally uniform cap layer has an average surface roughness less than about 1 nm.

79. A semiconductor structure comprising:

a semiconductor substrate;

a compositionally graded layer disposed over the substrate;

a substantially relaxed compositionally uniform cap layer disposed over the compositionally graded layer, wherein the cap layer has a density of dislocation pile-ups less than 1/cm.

80. The semiconductor structure of claim 79 wherein the cap layer has a density of dislocation pile-ups less than 0.01/cm.